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AMENDMENTS TO THE CLAIMS

1-25. (Cancelled)

26. (Previously Presented) A semiconductor device, comprising:

a metallic layer over a substrate;

a dielectric layer over said metallic layer;

a via hole extending through the dielectric layer to a surface of the metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole;

a second titanium aluminide layer or a titanium layer on sides of said via hole; and

a conductive material on the first titanium aluminide layer, said conductive material and said first titanium aluminide layer being in contact at an interface, said interface being substantially free from tensile stress between said first titanium aluminide layer and said conductive material.

27. (Previously Presented) A semiconductor device, comprising:

an aluminum layer over a substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining a bottom and sides of the via hole;

a titanium nitride layer over the titanium aluminide layer; and

a conductive plug material on the titanium nitride layer.

28. (Previously Presented) A semiconductor memory device, comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the semiconductor substrate;

an antireflective coating over said first metallic layer;

a second dielectric layer over the antireflective coating;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the first metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole;

a second titanium aluminide layer or a titanium layer on sides of said via hole;

a titanium compound containing layer on the first titanium aluminide layer and in contact with said first titanium aluminide layer at an interface that is substantially free of tensile stress;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the conductive plug material.

29. (Original) The semiconductor memory device as recited in claim 28, wherein the titanium compound layer is titanium nitride.

30. (Original) The semiconductor memory device as recited in claim 28, wherein the first metallic layer comprises aluminum.

31. (Original) The semiconductor memory device as recited in claim 28, wherein the memory circuit includes a SRAM cell.

32. (Original) The semiconductor memory device as recited in claim 28, wherein the memory circuit includes a DRAM cell.

33. (Previously Presented) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a first metallic layer over the semiconductor substrate;

an antireflective coating over the first metallic layer;

a dielectric layer over the antireflective coating;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium layer lining sides of the via hole;

a titanium compound containing layer over the titanium aluminide layer and the titanium layer, said titanium compound layer being in contact with said titanium aluminide layer, wherein said titanium compound layer experiences approximately no tensile stress from said titanium aluminide layer;

a conductive plug material formed over the titanium compound layer;

a second metallic layer on the dielectric layer and electrically connected to the conductive plug material; and

a connector on the semiconductor substrate and wired to said memory circuit.

34. (Previously Presented) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a metallic layer over the semiconductor substrate;

a dielectric layer over the metallic layer;

a via hole extending through the dielectric layer to a surface of the metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole;

a second titanium aluminide layer or a titanium layer lining sides of the via hole; and

a conductive material on the first titanium aluminide layer, wherein said conductive material and said first titanium aluminide layer are in contact at an interface having approximately no tensile stress from said first titanium aluminide layer; and

a connector on the semiconductor substrate and wired to said memory circuit.

35. (Previously Presented) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

an aluminum layer over the semiconductor substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining a bottom of the via hole;

a titanium layer lining sides of the via hole;

a titanium nitride layer substantially free of through cracks on the titanium aluminide layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said titanium aluminide layer and said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the conductive plug material; and

a connector on the semiconductor substrate and wired to said memory circuit.

36. (Previously Presented) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a memory circuit region in the semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer, said first metallic layer comprising aluminum;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer over the first metallic layer;

a via hole extending through the second dielectric layer to a surface of the first metallic layer;

a titanium aluminide layer lining a bottom of the via hole;

an aluminum plug on the titanium aluminide layer; and

a second metallic layer on the second dielectric layer and electrically connected to the aluminum plug material; and

a connector on the semiconductor substrate, said connector being wired to said memory circuit.

37. (Previously Presented) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a first metallic layer over a substrate;

a dielectric layer over the first metallic layer;

a via hole extending through the dielectric layer to a surface of the first metallic layer;

a titanium aluminide layer lining a bottom and sides of the via hole;

a titanium compound containing layer over the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer over the dielectric layer and electrically connected to the conductive plug material.

38. (Previously Presented) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a metallic layer over a substrate;

an antireflective coating over the metallic layer;

a dielectric layer over the antireflective coating;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the metallic layer;

a first titanium aluminide layer lining at least a bottom of the via hole;

a second titanium aluminide layer or a titanium layer lining sides of the via hole; and

a conductive material on the first titanium aluminide layer, wherein said conductive material is in contact with said first titanium aluminide layer at an interface, said interface being substantially free of tensile stress between said first titanium aluminide layer and said conductive material.

39. (Previously Presented) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

an aluminum layer over a substrate;

a dielectric layer over the aluminum layer;

a via hole extending through the dielectric layer to a surface of the aluminum layer;

a titanium aluminide layer lining a bottom of the via hole;

a titanium layer lining sides of the via hole;

a titanium nitride layer substantially free of through cracks on the titanium aluminide layer and the titanium layer, wherein said titanium nitride layer is in contact with said titanium aluminide layer and said titanium aluminide layer exerts approximately zero tensile stress upon said titanium nitride layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the conductive plug material.

40. (Previously Presented) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer, said first metallic layer comprising aluminum;

a contact interconnect between the first metallic layer and the semiconductor substrate;

an antireflective coating over the first metallic layer;

a second dielectric layer over the antireflective coating;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the first metallic layer;

a titanium aluminide layer lining a bottom and sides of the via hole;

a conductive plug material on the titanium aluminide layer, said conductive plug material comprising aluminum; and

a second metallic layer on the second dielectric layer and electrically connected to the conductive plug material, said second metallic layer comprising aluminum.